Introducing and validating new formats for IP design using Fractal Crossfire

A Fractal Whitepaper

Introduction

Semiconductor design automation has always been very dynamic in terms of models, descriptions and design tools. A natural consequence from Moore's law is that with every new manufacturing node, not only the complexity of the designs increases but also that new physical effects need to be modeled to avoid expensive silicon debugging and design re-spins. Combine this with a healthy level of competition, and it becomes clear that IP or library characterization flows can never be copied as-is to a next manufacturing node.

New formats and databases need to be included in the IP deliverables, with the same amount of quality and robustness as the existing, proven formats. Fractal Crossfire is an IP quality assurance tool, used by IP design teams and SoC designers, to verify the consistency and quality of a particular IP delivery. Crossfire's unique common data-model allows different databases and formats to be cross-checked for completeness against a golden reference format or against a previous release. In addition Crossfire provides a rich set of quality assurance checks to dive deeper into the models provided by the different formats such as trend-checks for timing and power values across process corners.

In this note the process by which Crossfire supports the introduction of new formats in IP design is described and is illustrated by a few recent additions to the formats supported by Crossfire will be described. These include APL (Apache's Power Library), UPF (Unified Power Format), CTL (Core Test Language) and AOCVM (Advanced On Chip Variability Model).

Introducing and checking new formats

When an IP characterization flow needs to be extended with a new format to be included in the final delivery, two phases can be distinguished in the path to maturity. These are illustrated in the following figure.

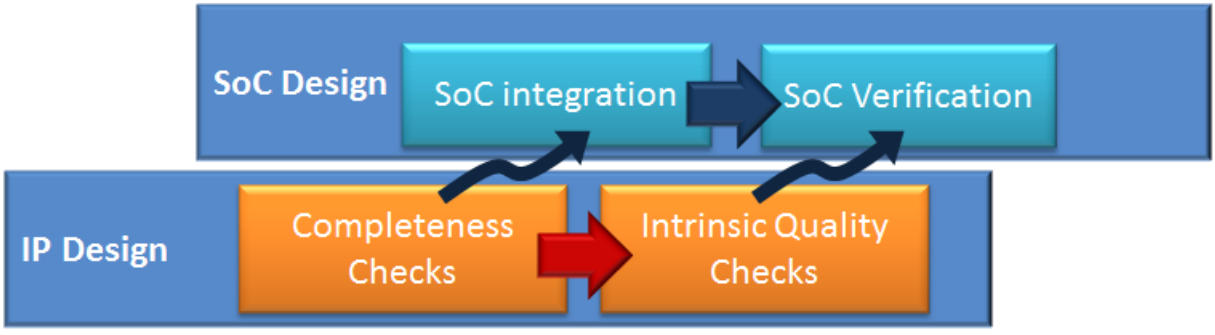

Figure 1, New format introduction and validation

Completeness phase

In this first phase the completeness of the new models needs to be assured. Without making sure a new format contains everything it should contain, more advanced checks are not very useful as the errors found are very likely consequences of missing items. The Crossfire completeness checks will compare any item that has been parsed to equivalent items from a reference. These checks apply to all different object types in the Crossfire data model, such as cells, pins, nets, timing arcs, but also to power domains.

When integrating a new format in the IP characterization, completeness is the first concern of the design team. Once a new format can be proven complete, this means that it's generation is well integrated into the automated characterization flow. So when the IP is extended with e.g. new cells or process corners, these will be correctly and automatically included in the new format as well.

Intrinsic quality phase

In this next phase the intrinsic quality of a format will be checked. Checks in this category ensure that the values describing, e.g. the timing or power characterization, make sense from a physical perspective. Crossfire will for example take the various process corners described in .lib files and check whether delays will indeed increase with rising substrate temperature or decrease with increasing supply voltage. For the IP characterization team these are issues concerning the detailed modeling, e.g. SPICE simulations, for the format itself, no longer in relation to the other formats in the library.

For SoC designers, these 2 phases are relevant in that after Crossfire has validated the completeness phase, a first release of the IP for integration purposes can be made available. This allows many parts of the SoC design flow to be tested, as all the necessary IP formats are available and complete. Only the final verification of the SoC before tape-out requires Crossfire sign-off of the intrinsic quality phase.

Recent Crossfire format additions

This section describes a number of recent format additions to the Crossfire product, their purpose and the relevant checks.

- APL
  The Apache Power Library is a binary format which serves as input to Apache's RedHawk product (now Ansys) for voltage-drop and reliability verification. APL models all power aspects of a particular cell or IP, including power domains, switching currents and parasitics. Besides completeness checks for cells and power-pins, Crossfire also contains trend checks for APL for instance by checking for increasing currents at increasing output loads.

- UPF
  The Unified Power Format is input to the Synopsys design tools for calculating power budgets. Like APL, only power pins are described in UPF. The purpose of UPF is to describe the power intent of the entire design: power domains, voltages and related pin names. The UPF power domains have to be physically separated networks in the

IP design. Crossfire is able to verify this requirement by cross-checking UPF against the SPICE netlist. Once the UPF vs. SPICE has proven to be complete, i.e. all cells and power pins are present, Crossfire is able to trace the SPICE netlists for every power domain and ensure they are separated.

The power domain separation test scales from cell to IP level. For example, for a 2GB SPICE file describing roughly 50 M transistors, analyzing the power domains in Crossfire takes only 5 minutes.

- CTL
  The Core Test Language is an IEEE standard for describing the Design For Test interfaces of a particular IP. This includes the terminals denoting scan-chains and test-control pins. For these pins, Crossfire is able to check consistent naming and functionality.

- AOCVM
  The Advanced On Chip Variability Format is a Liberty extension aimed at modeling the variation of cell-delays during manufacturing. This variation of cell delays can impact timing correctness in 2 ways: increasing delays may lead to designs no longer reaching the required speeds - and thus to yield loss. A second mechanism is that shorter cell delays on certain critical paths may lead to too early signal arrival times, which compromises the functionality of the design. AOCVM models a simplified model for the probability of cell delay variation which takes in to account the location of the cell on the wafer and the logic depth. Statistical static timing analysis tools will then predict the fraction of yield loss due to these effects.

  For AOCVM Crossfire carefully checks the completeness and consistency against the available Liberty models for timing and power. Also, Crossfire checks for trends in AOCVM, for instance by checking for a reduced variability of delays with increasing logic depth.

Crossfire versatility

Key to the above mentioned recent additions to Crossfire is its versatility. Currently Crossfire supports a total of 40 different formats and databases for completeness and intrinsic quality checking. When new formats emerge, they are included in the Crossfire portfolio in a matter of weeks, or shorter when public domain parsers are available. After parsing, completeness checks are instantly available in Crossfire thanks to the common data model. This allows IP design teams to quickly bring a new format on-stream in their characterization flows, and avoids having their customers suffer from trivialities like missing pins during the first integration runs.

Another illustration of this versatility is the generic PDF reader that is part of the Crossfire offering. The PDF reader is a generic software component that allows end-users to parse their own proprietary datasheets into the Crossfire common data-model and thus also check the documentation for completeness.

Versatility is also available on the level of intrinsic quality checks. Crossfire offers a flexible API that allows users to code proprietary checks on their IP. As all information contained in

the individual formats is also available in the common data-model, custom checks can be coded and added to the GUI for end-users easily.

Conclusion

Recent format additions to Fractal Crossfire have been described for APL, UPF, CPL, and AOCVM. These new formats serve as illustrations for the different checks designers need from a quality assurance tool like Crossfire. First, completeness checks are required in a very early stage of development to enable IP integration runs. These are followed by intrinsic quality checks on the individual formats in subsequent IP releases to support the final SoC verification. After the completeness phase has been signed off by Crossfire, a first IP release allows the IP design and the SoC design integration teams to work in parallel.